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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/037,191	01/04/2002	Peter Schulter	112153.129	6693

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EXAMINER	
PIERRE LOUIS, ANDRE	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 07/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/037,191	SCHULTER ET AL.	
	Examiner	Art Unit	
	Andre Pierre-Louis	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07/29/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claim 1-20 have been presented for examination.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1-4, 9 and 11-14,19 are rejected under 35 U.S.C. 102(b) as being anticipated by Aditya (*U.S. Patent No. 5,918,021)*.

1.1. In considering the independent claims 1 and 11, Aditya reference teaches the emulation of a switched Ethernet local area network in a platform having a plurality of computer processors, a switch fabric and point-to-point links to the processors (see figure 3); in particular, he teaches the steps of:

- providing Ethernet driver emulation logic to execute on at least two computer processors; (*figure 2 (126)*).
- providing switch emulation logic to execute on at least one of the computer processors; (*figure 1 (150)*).
- establishing a virtual interface between the switch emulation logic and each computer processor having Ethernet driver emulation logic executing thereon to allow software communication therebetween, wherein each virtual interface defines a software communication path from one

computer processor to another computer processor via the switch fabric; (*col.1 line 64 through col.2 line 6*)

- establishing a virtual interface between each computer processor having Ethernet driver emulation logic executing thereon and every other computer processor having Ethernet driver emulation logic executing thereon; (*col. 2 line 1-6*)

if the virtual interface between one computer processor and another is operating to satisfy predetermined criteria, the Ethernet driver emulation logic of the one computer processor unicast communicating with the other computer processor via a virtual interface defining a software communication path therebetween;(*col.6 lines 50-60).*

if the virtual interface between one computer processor and another is operating to not satisfy predetermined criteria, the Ethernet driver emulation logic of the one computer processor unicast communicating with the other computer processor via a virtual interface to the switch emulation logic which transmits the unicast communication to the other computer processor (*col. 6 lines 60-61*).

1.2. As per claims 2 and 12, Aditya reference teaches the functional equivalent of an Ethernet driver emulation associated with a virtual MAC address wherein the MAC addresses are formed according to rules to identify the computer processor as one of the plurality of computer processors distinct from that of the external network (*col.5 line 15-17*).

1.3. With regards to claims 3 and 13, Aditya reference discloses that the platform is connected to an external network via interface logic for communicating with

an external network interface is associated with its own MAC address, and wherein messages are communicated on the external network using the MAC address of the external network interface logic (*col. 5 lines 17-21*).

1.4. With regards to claims 4 and 14, the Aditya reference inherently teaches the use of different virtual interface for communication between multiple computer processors ((*see fig. 2 (141) col. 5 lines 15-17*)) as each NIC possesses its own MAC address (*col.1 lines 60-62*).

1.5. As per claims 9 and 19, the Aditya reference teaches a switch emulation logic that defines and maintains computer processor membership (*col.6 lines 24-30*).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

2. Claims 5-7 and 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aditya (*U.S. Patent No. 5,918,021)* as applied to claims 1-4,9 and 11-14,19 above, and further in view of Hebert (U.S. Patent No. 6,728,780).

2.1. In considering claims, 5 and 15, Aditya reference teaches the check summing capability (*fig. 6 col. 5 line 38-43*), but it does not teach the disabling of such check summing. However, Hebert teaches the disabling of such check summing if the switch fabric driver logic has already check summed a message (see Hebert col.2 lines 51-59). It would have been to one ordinary skill of the art to have modified Aditya's by adding the check summing disablement so that the system does not check sum a message that has already been check summed.

2.2. With regards to claims 6 and 16, Aditya reference teaches most of the claims limitations; but does not teach the reliable communication protocol. However, Hebert reference teaches the use of a reliable communication protocol to ensure reception of message over the switch fabric (*see Hebert col.5 lines 12-17).*

Thus it would have been obvious for one ordinary skill in the art at the time of applicant's invention to have modified Aditya's system by adding the reliable communication protocol to ensure that messages get to its destination.

2.3. With regards to claims 7 and 17, the combination of Aditya and Hebert references disclose the redundant configuration (*see Hebert figure 3 col. 4 lines 56-57*).

3. Claims 8,10, 18 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aditya as applied to claims 1-7,9 and 11-17,19 above, and further in view of Trachewsky et al (U.S. Patent No. 6,898,204).

3.1. With regards to claims 8 and 18, Aditya reference teaches most of the claims (*see figure 3*); however it does teach the switch emulation logic receiving and cloning the broadcast message from the virtual interface and transmitting it to the other computer processors in the network. On the other hand, Trachewsky et al reference teaches the use of an Ethernet emulation logic to broadcast communicate a message by sending the message to the switch emulation logic via a virtual interface as the switch emulation logic receives and clones the broadcast message from a virtual interface and transmits it the other computer processors in the network (*col.29 line 60 through col.30 line 58*). Thus it would have been obvious to one ordinary skill in the art at the time of applicant's invention to modify Aditya's system by adding the cloning feature to Aditya's system in other to retrieve these messages and send them to other computer processors in the network.

3.2. In considering claims 10 and 20, the combination of aditya and Trachewsky et al references discloses the transmission capability of a switched Ethernet driver emulation logic of more than the maximum transmission unit (MTU) (see *Trachewsky et al col. 29 line 60 through col. 58).*

Conclusion

Claims 1-20 are rejected and this action is non-final.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andre Pierre-Louis whose telephone number is 571-272-8636. The examiner can normally be reached on Mon-Fri, 8am-4: 30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo P. Picard can be reached on 571-272-3749. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

APL
July 8, 2005

JEAN R. HOMERE
PRIMARY EXAMINER